

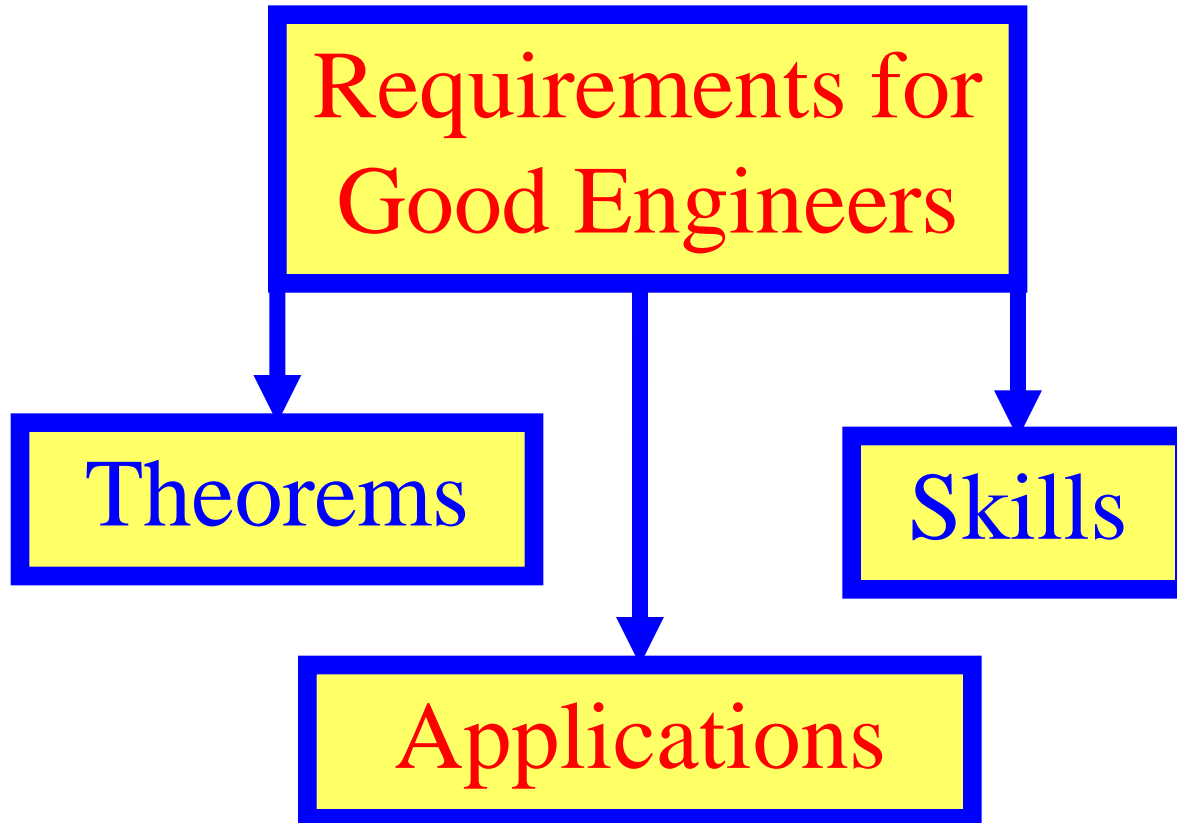


Introduction to Programmable Logic

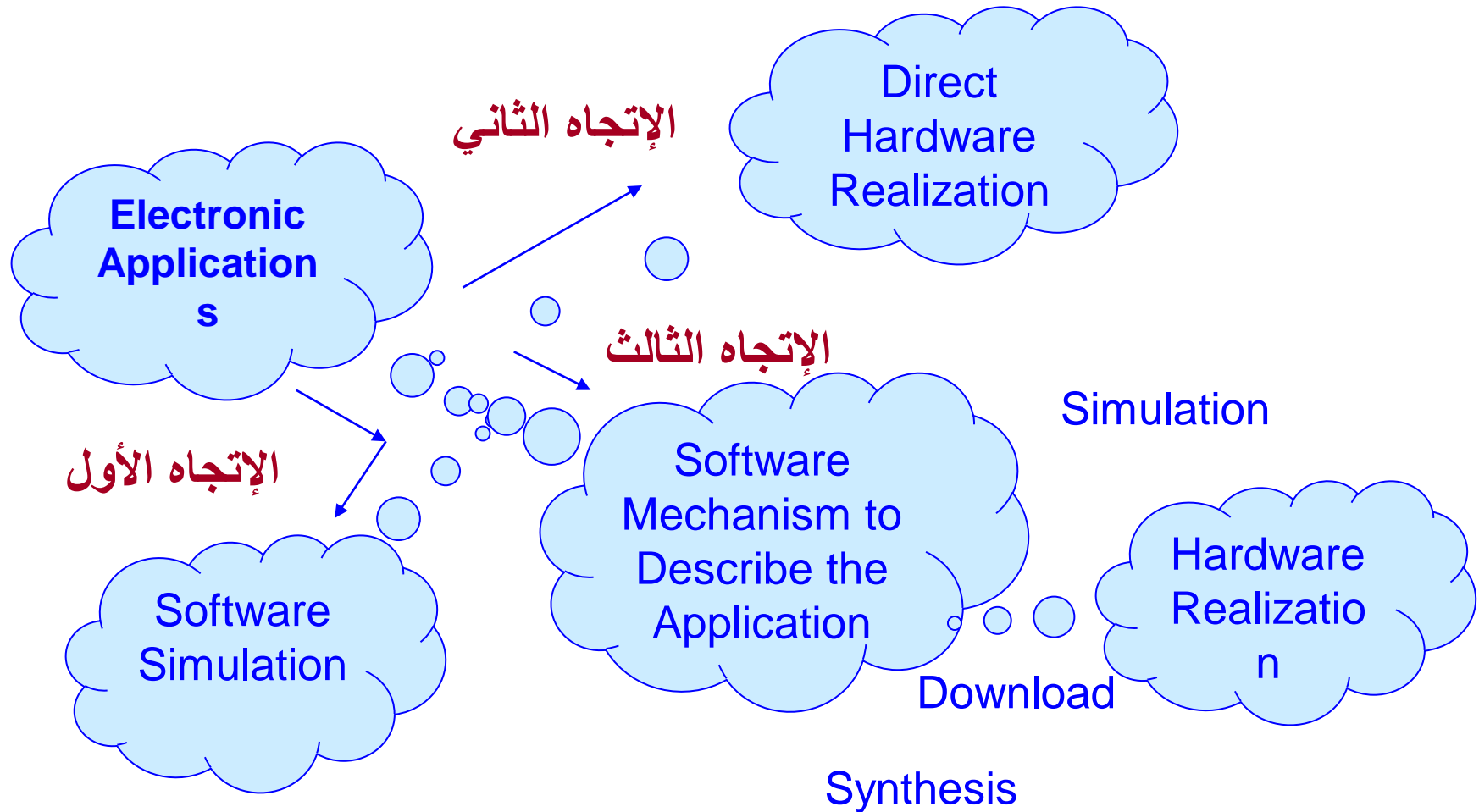


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Introduction



Introduction



Introduction (Cont'd)

■ الإتجاه الأول:

- ◆ The output was pure software.
- ◆ No physical products.
- ◆ Even if we consider this software as a product; actually it is a slow realization of the required application.
- ◆ Low cost.

■ الإتجاه الثاني:

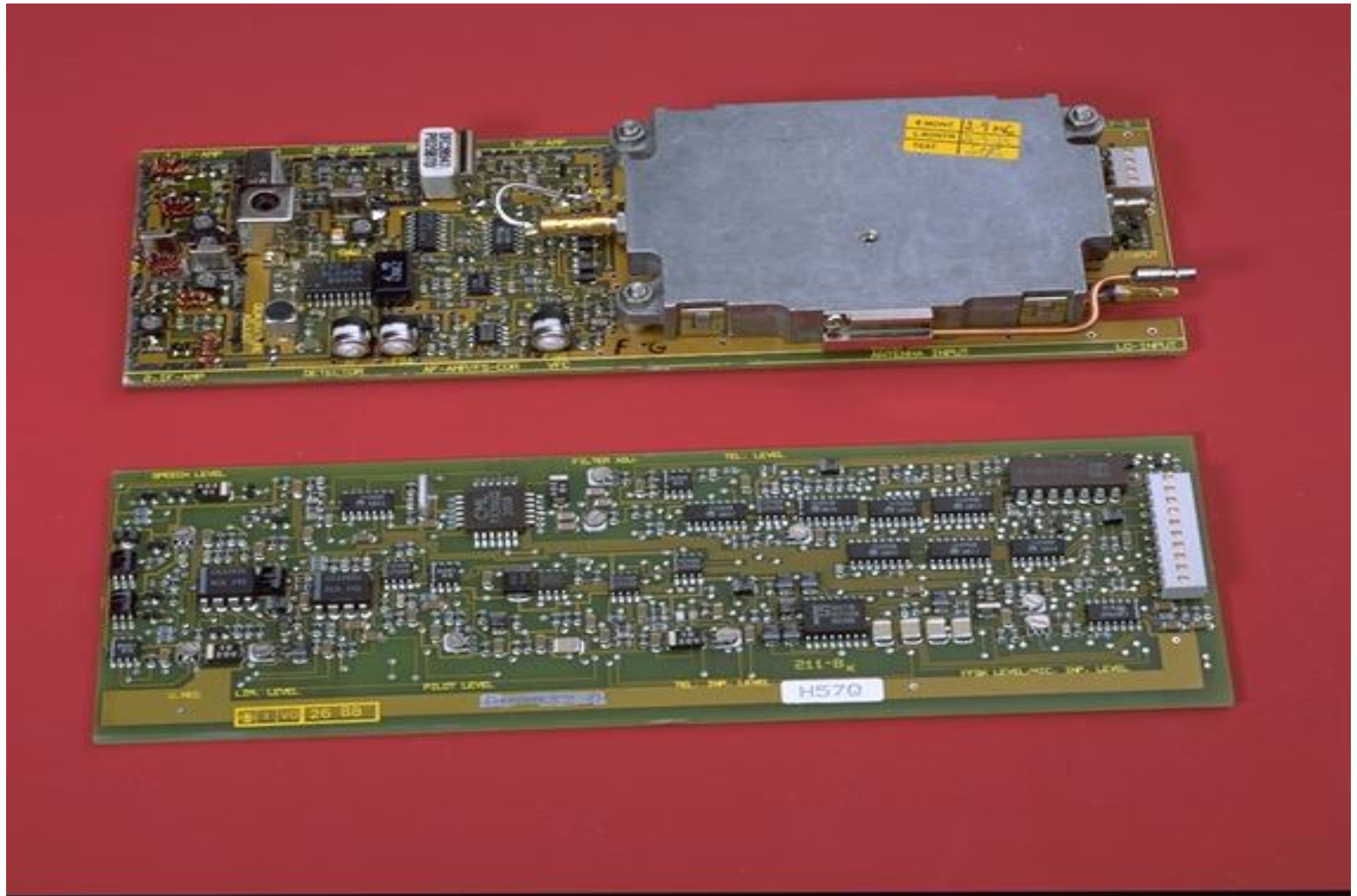
- ◆ The output was pure hardware.
- ◆ No specialized skills are required except:
 - ☞ Simple computer programs to draw the layout.
 - ☞ Simple computer programs to simulate the application.
 - ☞ Simple Wiring and Welding skills.
- ◆ The output product may be as shown below for the most clever engineers.
- ◆ Fairly high cost
- ◆ Fixed design.

Introduction (Cont'd)

■ الإتجاه الثاني:

- Draw the schematic diagram of the application and simulate it using simple computer programs:
 - ◆ PSpice.
 - ◆ Multisim.
- Draw the layout manually or using simple computer programs:
 - ◆ PSpice.
 - ◆ Eagle.
 - ◆ PCB123.
 - ◆ PCB Express.
- Print the layout over a calk paper.
- Using the Silk Screen Technology or the Ultra Violet to a copper sheet coated with a photo-resist material.
- Etching using some acids.
- Washing to remove acid effects.
- Using drill to open component holes.
- Place the components.
- Soldering these components.

Introduction (Cont'd)



Introduction (Cont'd)

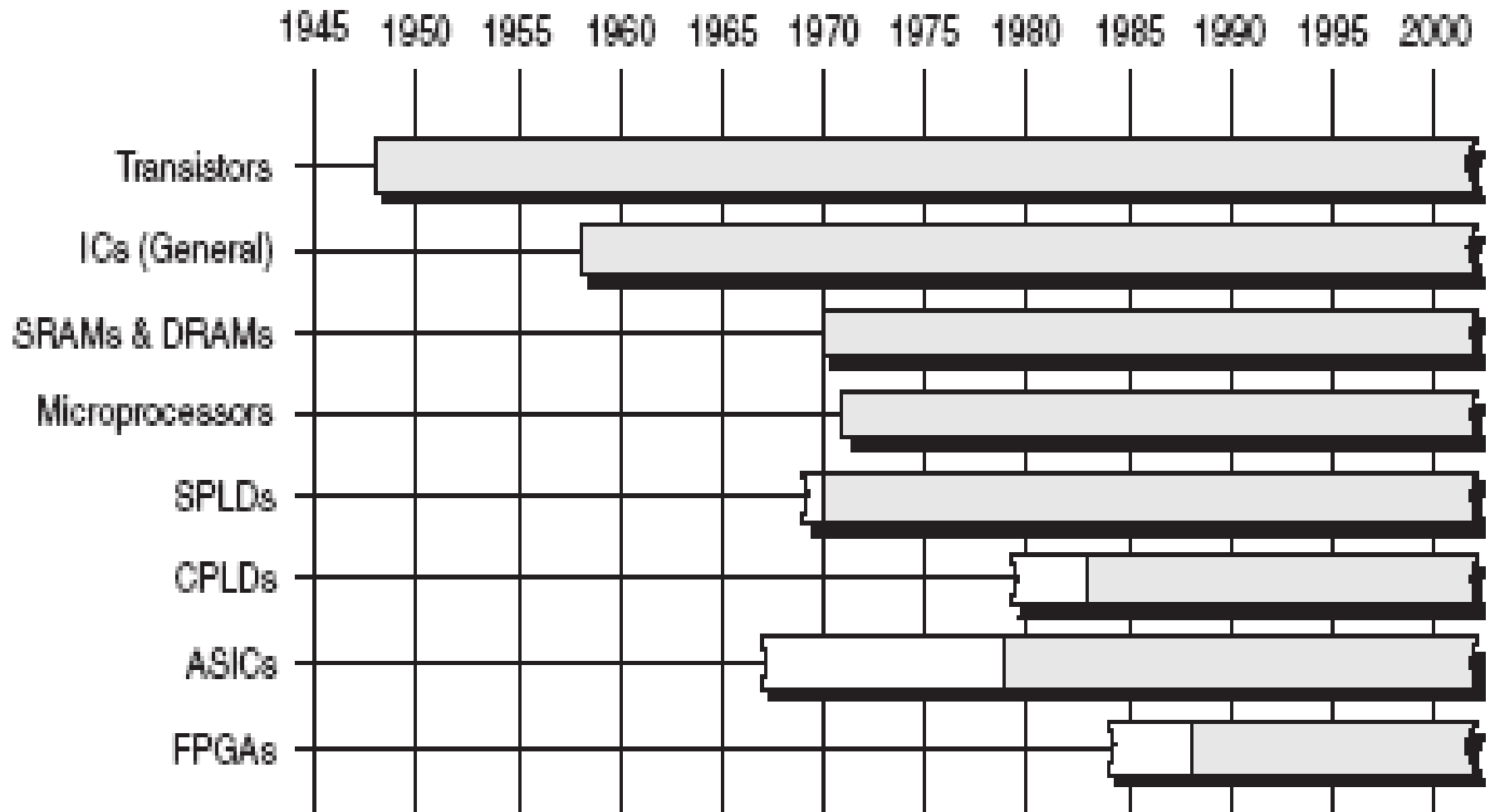
■ الإتجاه الثالث:

- ◆ Requires high level skills.
- ◆ Fairly high cost.
- ◆ Requires both software and hardware skills.
- ◆ Covers huge number of engineering applications.
- ◆ Sometimes produces new products for new and/or old applications.
- ◆ Simplify the hardware realization of many complex applications.



Programmable Chip

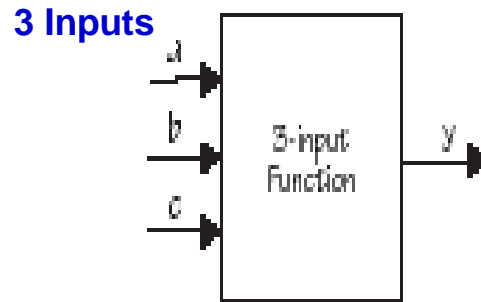
Technology Timeline



Technology Overview

1. Fixed Logic

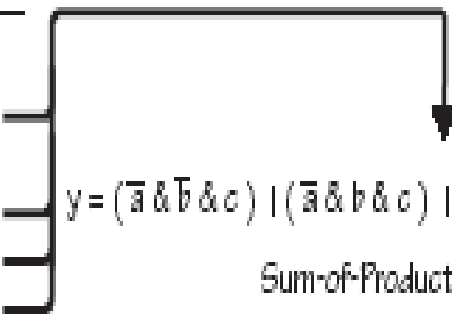
Black Box



Truth Table

a	b	c	y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

SUM of PRODUCTS

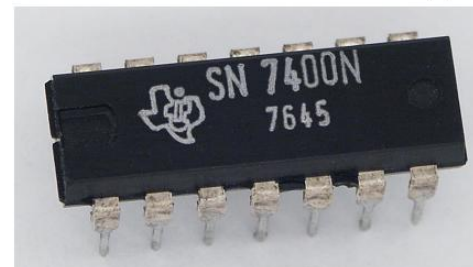
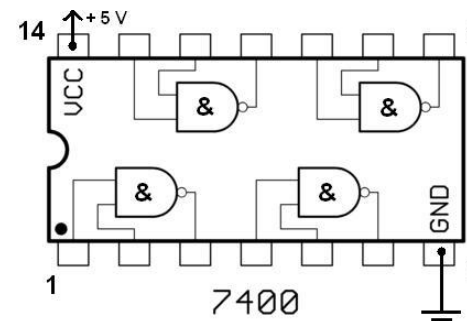

$$y = (\bar{a} \& \bar{b} \& c) \mid (\bar{a} \& b \& c) \mid (a \& \bar{b} \& \bar{c}) \mid (a \& \bar{b} \& c)$$

Sum-of-Products Expression

Application

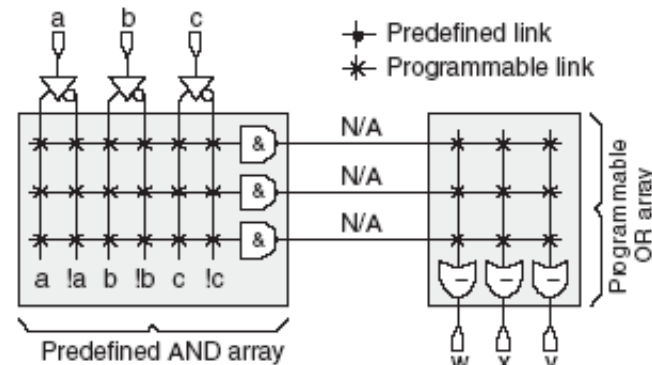
Connect Standard Logic Chips
Very Simple Glue Logic

Logic Expression



2. Programmable Logic Devices “PLDs”

- Different Types
- SUM of PRODUCTS
- Prefabricated
- Programmable Links
- Reconfigurable



Un-programmed State

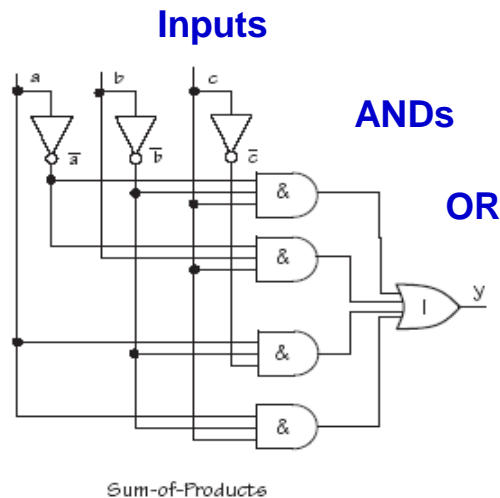
Planes of
ANDs, ORs

$$y = (a \& b \& c)$$

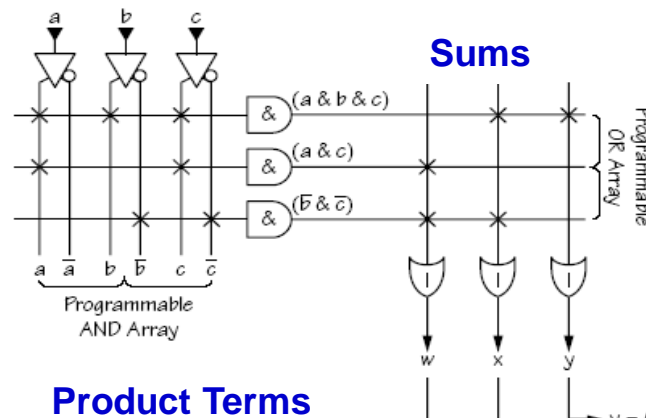
$$x = (a \& b \& c) \mid (\bar{b} \& \bar{c})$$

$$w = (a \& c) \mid (\bar{b} \& \bar{c})$$

Logic Function



Sum of Products



Programmed PLD

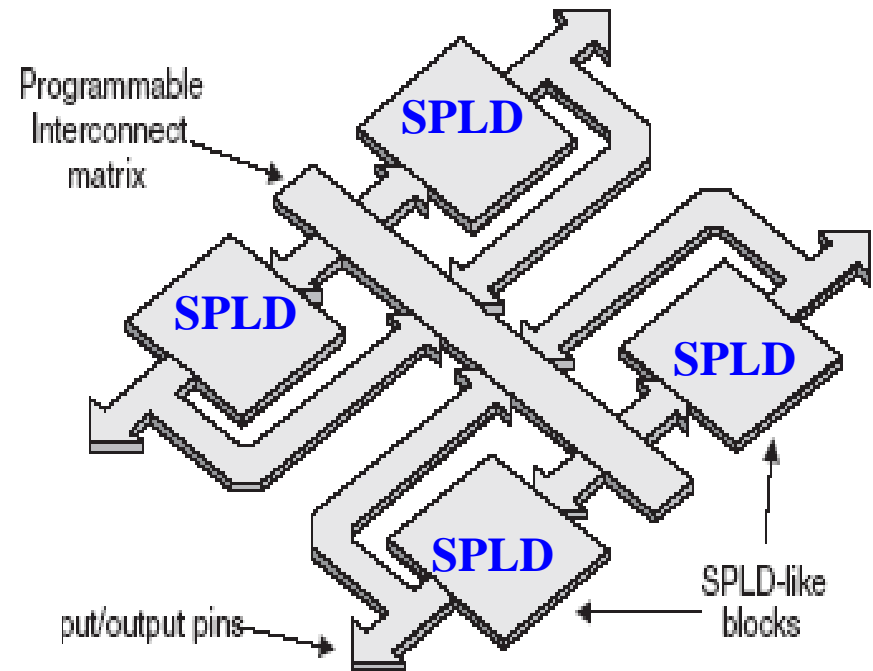
$$y = (a \& b \& c)$$

$$x = (a \& b \& c) \mid (\bar{b} \& \bar{c})$$

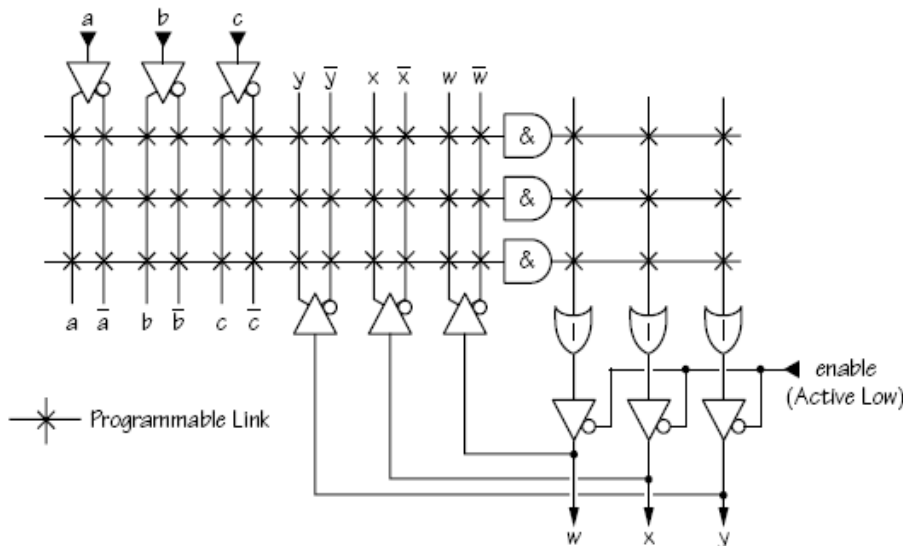
$$w = (a \& c) \mid (\bar{b} \& \bar{c})$$

3. Complex PLDs

- CPLDs
- Programmable PLD Blocks
- Programmable Interconnects
- Electrically Erasable links



CPLD Architecture

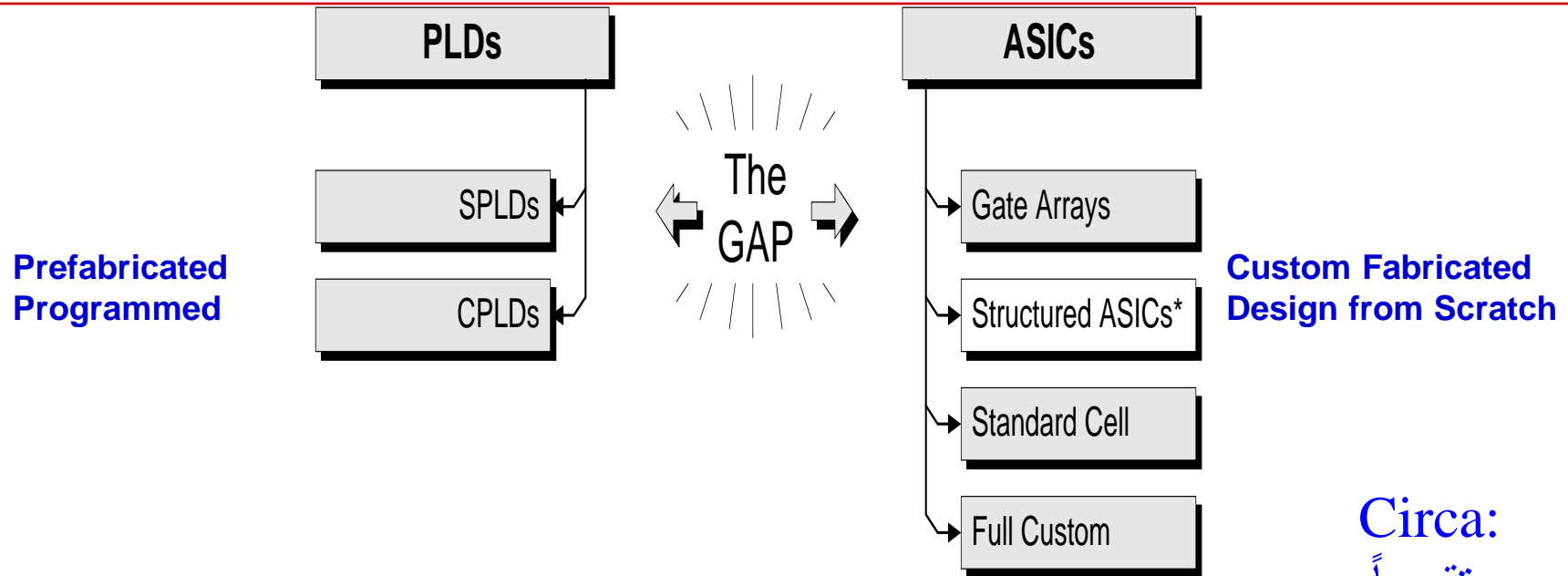


Feedback Outputs

4. Application Specific Integrated Circuits (ASIC)

- An ASIC is an IC customized for a particular use, rather than intended for general-purpose use.
- For example, a chip designed solely to run a **cell phone** is an ASIC.
- ASIC Features:
 - ◆ Large Complex Functions.
 - ◆ Millions of Gates
 - ◆ Customized for Extremes of Speed, Low Power,
 - ◆ (Very) Expensive (in small quantities) > \$1 Million mask set
 - ◆ (Very) Hard to Design.
 - ◆ Long Design cycles.
 - ◆ NOT Reprogrammable.
 - ◆ High Risk

Application Specific Integrated Circuits “ASICs”



*Not available circa early 1980s

Circa:
تقريباً

advantages

disadvantages

Limited Complexity
Thousands of Gates

advantages

Cheap
Easy to Design
Reprogrammable.

Large Complex Functions.

Millions of Gates

Customized for Extremes of Speed, Low Power,

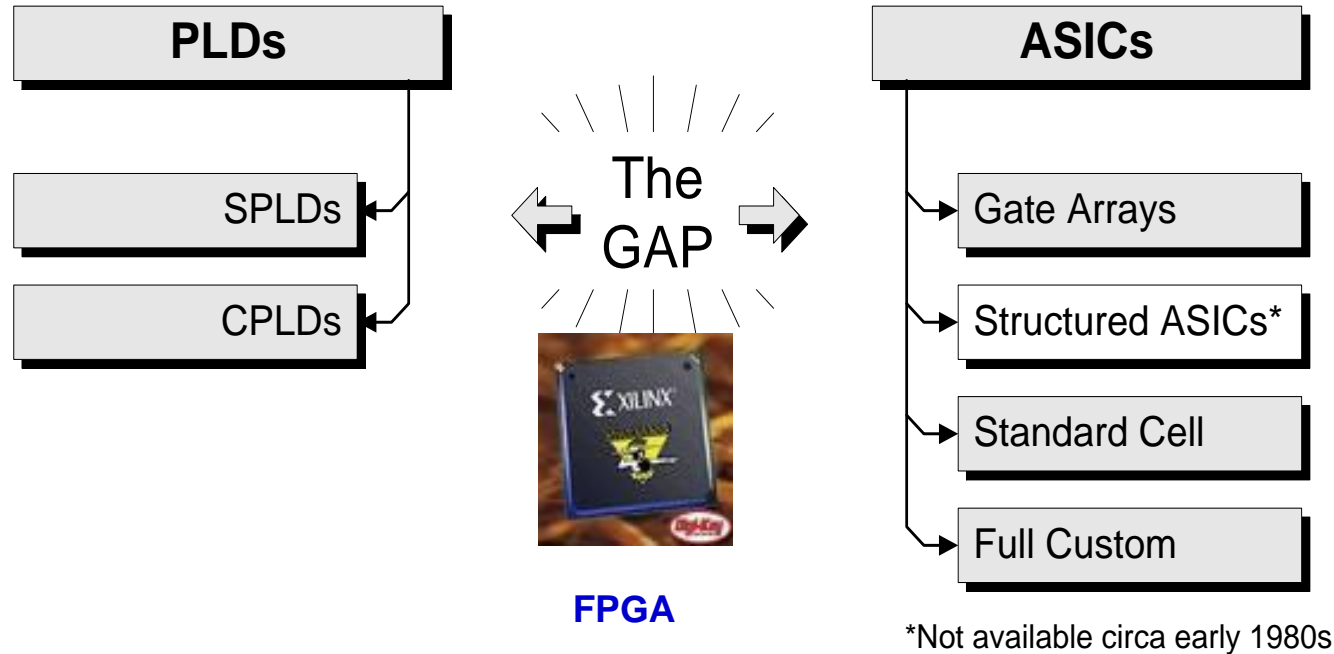
(Very) Expensive (in small quantities) > \$1 Million mask set

(Very) Hard to Design.

Long Design cycles.

NOT Reprogrammable. High Risk

Application Specific Integrated Circuits “ASICs”

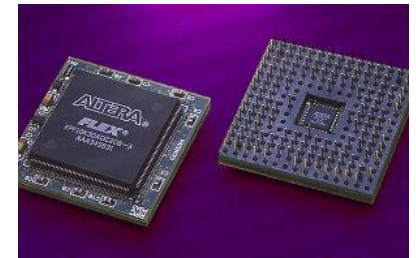


Inexpensive
Easy to Design
Reprogrammable.

Large Complex Functions

Field Programmable Gate Arrays “FPGA”

- **Field Programmable Gate Array**
 - ◆ New Architecture
 - ◆ ‘Simple’ Programmable Logic Blocks
 - ◆ Massive Fabric of Programmable Interconnects

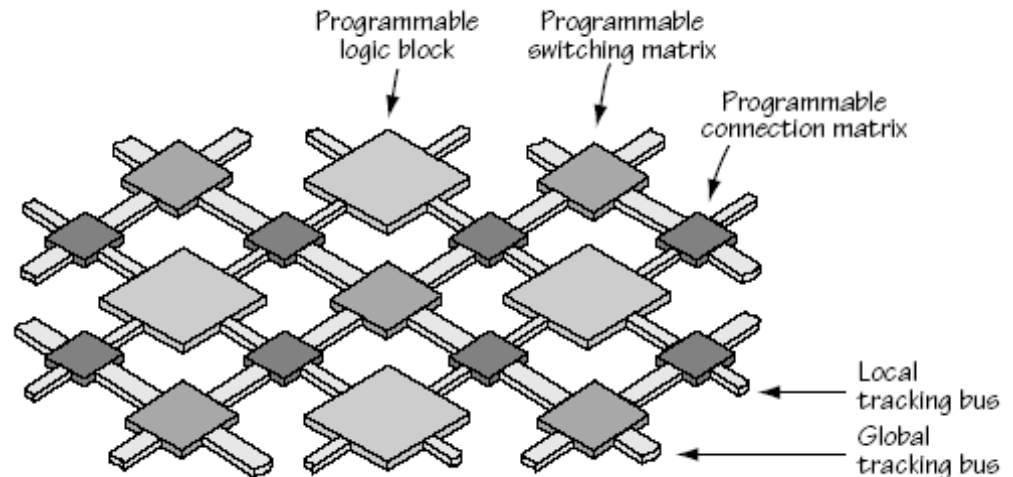


Large Number of Logic Block ‘Islands’

1,000 ... 100,000+

in a ‘Sea’ of Interconnects

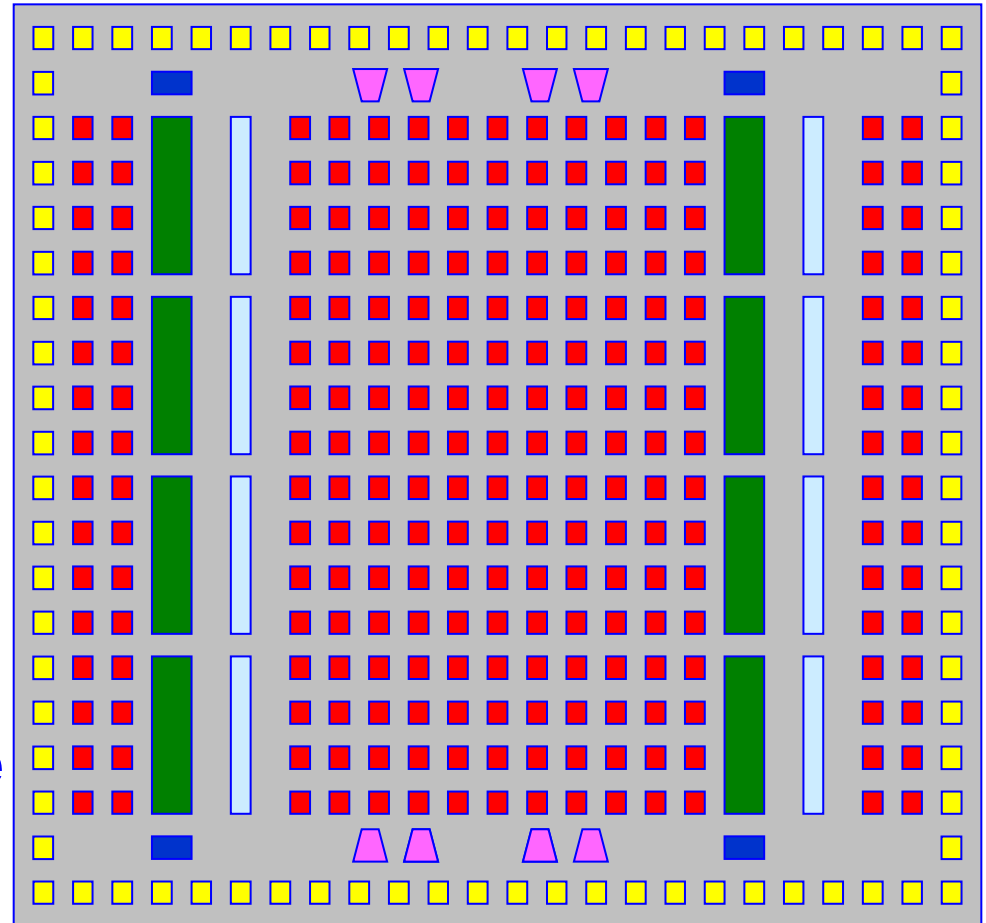
FPGA Architecture



5. Field Programming Gate Array (FPGA) Technology

Xilinx FPGA Architecture

- **Logic Fabric (بنية)**
 - ◆ Gates and flip-flops
- **Embedded Blocks**
 - ◆ Memory
 - ◆ DSP/Multipliers
 - ◆ Clock management
 - ◆ High speed serial I/O
 - ◆ Soft/hard processors
- **Programmable I/Os**
- **In-system programmable**



Logic Fabric

- **Logic Cell**

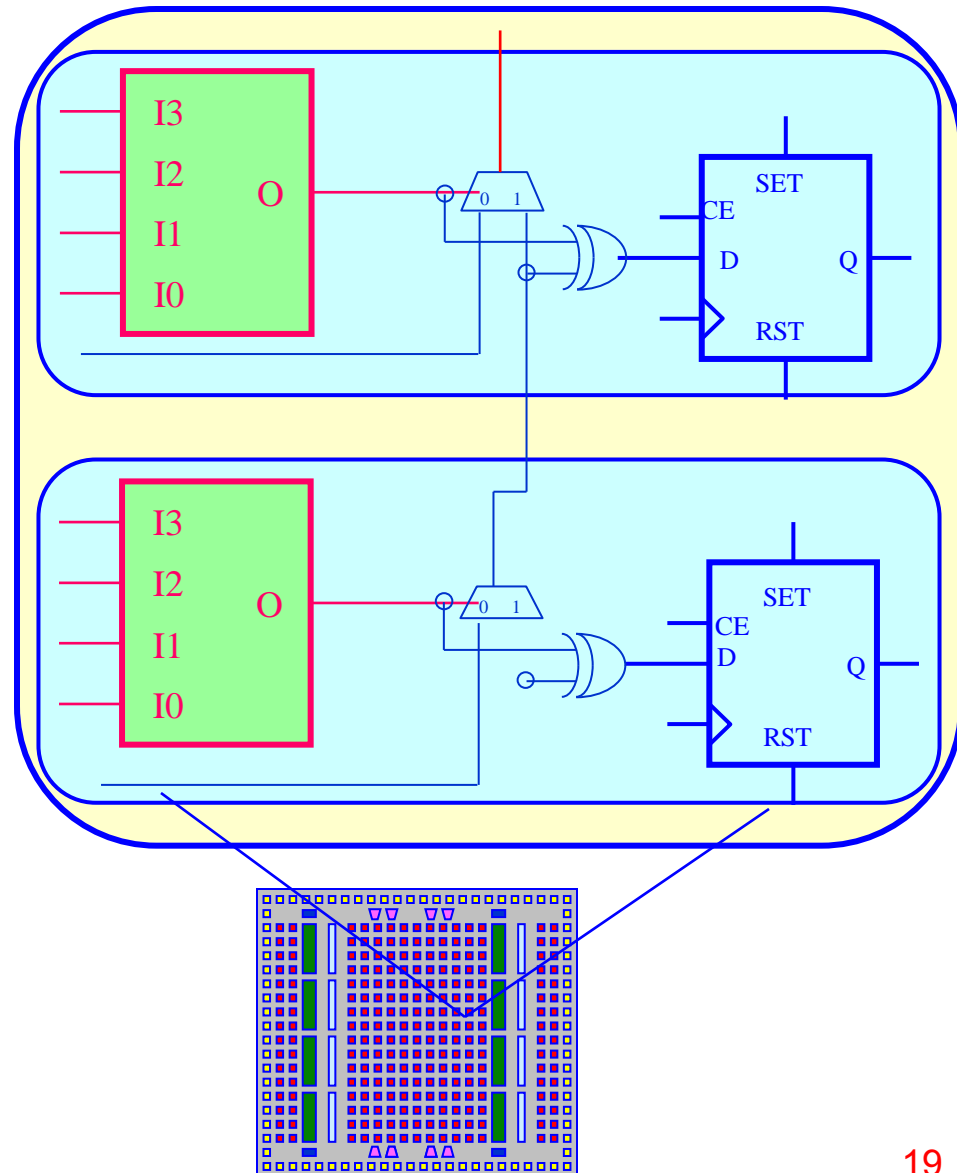
- ◆ Lookup table (LUT)
- ◆ Flip-Flop
- ◆ Carry logic
- ◆ Muxes (not shown)

- **Slice**

- ◆ Two Logic Cells

- **Spartan-3E FPGAs**

- ◆ 2K to 33K logic cells

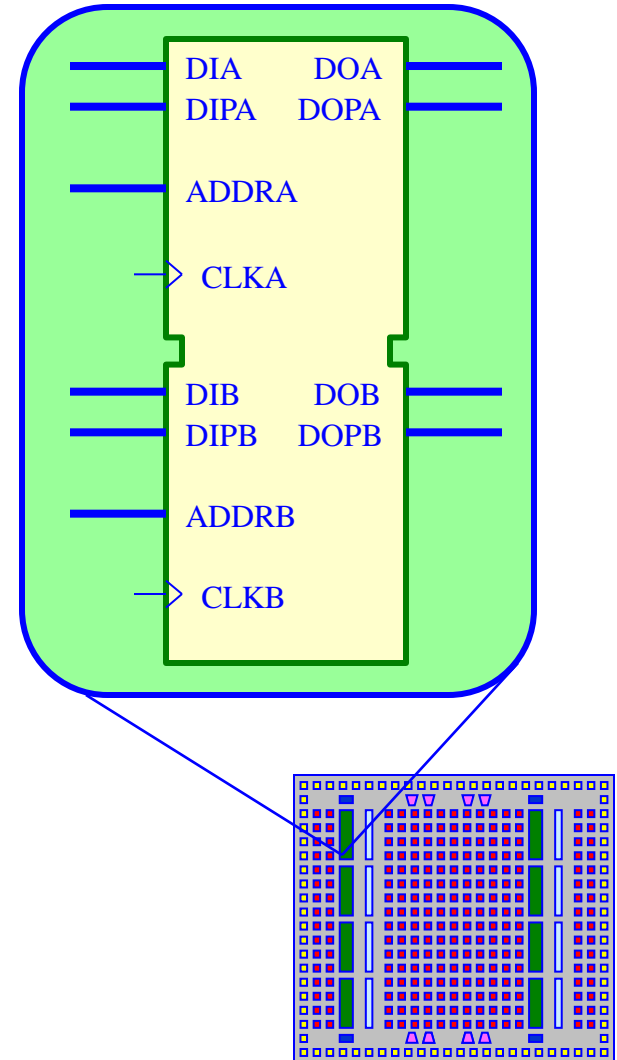


Memory

■ Block RAM

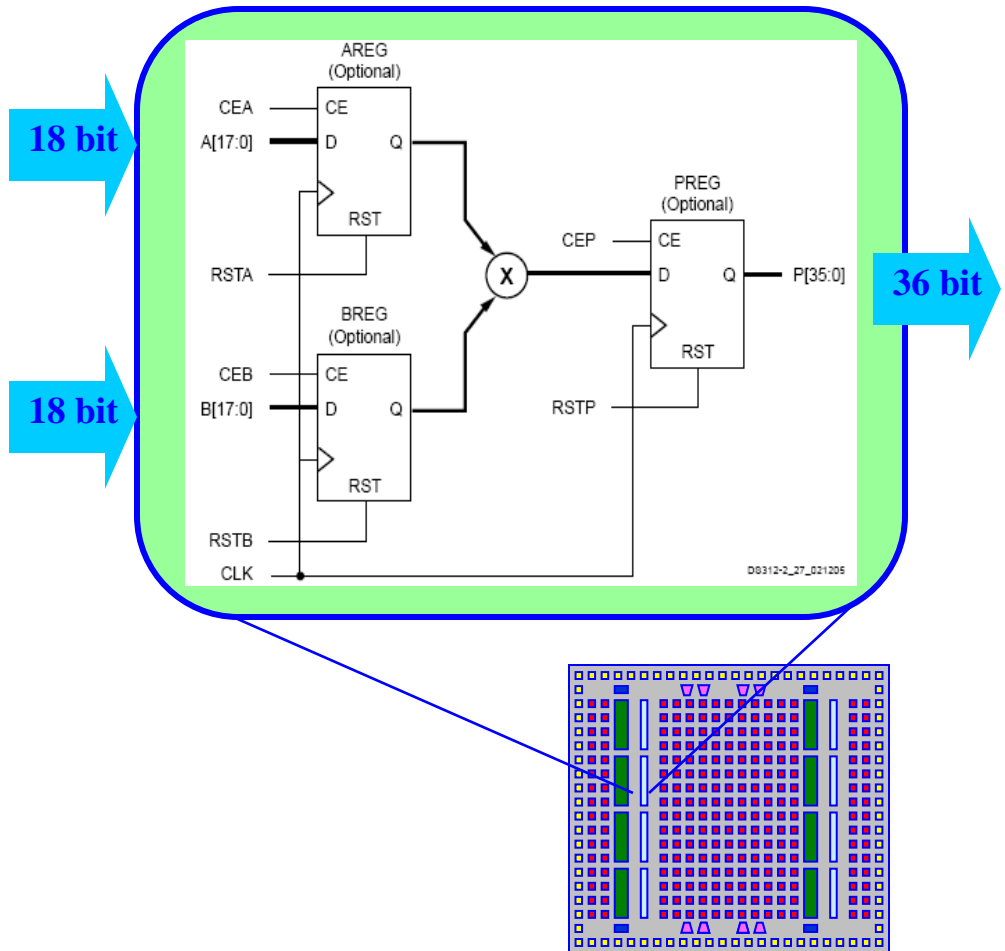
- ◆ RAM or ROM
- ◆ True dual port
 - ☞ Separate read and write ports
- ◆ Independent port size
 - ☞ Data width translation
- ◆ Excellent for FIFOs

Block RAM Configurations			
Configuration	Depth	Data bits	Parity bits
16K x 1	16Kb	1	0
8K x 2	8Kb	2	0
4K x 4	4Kb	4	0
2K x 9	2Kb	8	1
1K x 18	1Kb	16	2
512 x 36	512	32	4



Multipliers

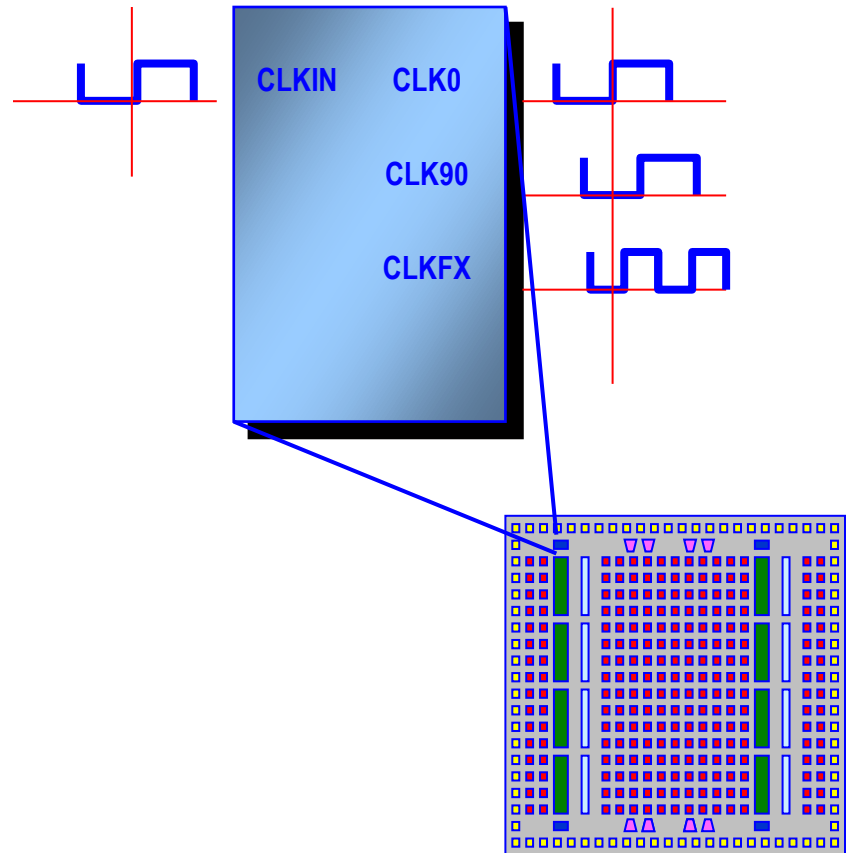
- **18 x 18 Multipliers**
 - ◆ Signed or unsigned
 - ◆ Optional pipeline stage
 - ◆ Cascadable



Clock Management

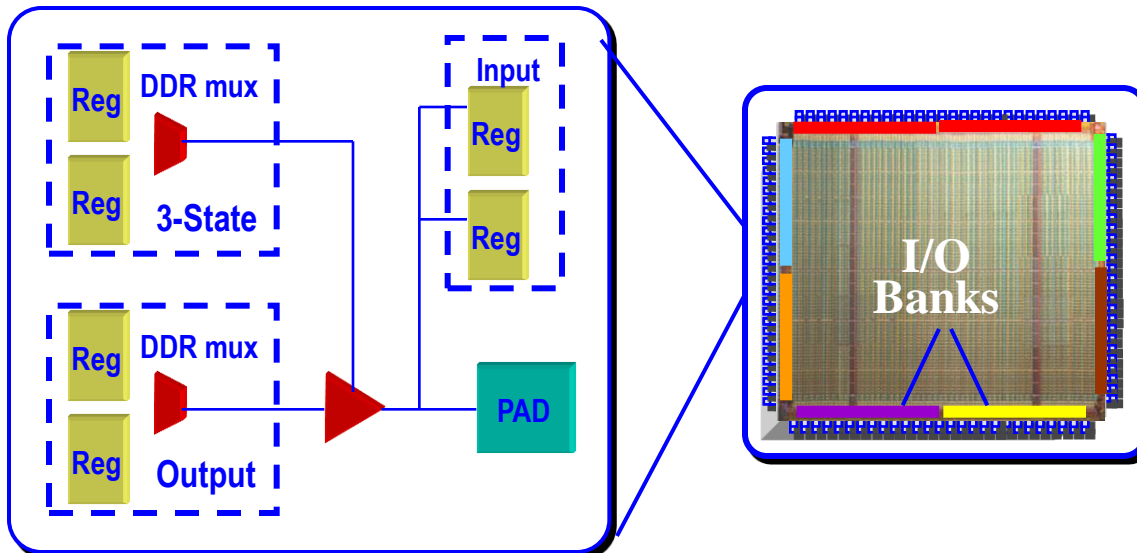
■ Digital Clock Managers (DCMs)

- ◆ Clock de-skew
- ◆ Phase shifting
- ◆ Clock multiplication
- ◆ Clock division
- ◆ Frequency synthesis



Programmable I/Os

- Single-ended
- Differential / LVDS
- Programmable I/O standards
 - ◆ Multiple I/O banks
- DDR I/O registers
- On-chip termination



	Standard	Output V_{CCO}	Input V_{REF}
Single ended	LVTTL	3.3V	--
	LVC MOS33	3.3V	--
	LVC MOS25	2.5V	--
	LVC MOS18	1.8V	--
	LVC MOS15	1.5V	--
	LVC MOS12	1.2V	--
	PCI 32/64 bit 33MHz	3.3V	--
	SSTL2 Class I	2.5V	1.25V
	SSTL2 Class II	2.5V	1.25V
	SSTL18 Class I	1.8V	0.9V
	HSTL Class I	1.5V	0.75V
	HSTL Class III	1.5V	0.9V
	HSTL18 Class I	1.8V	0.9V
	HSTL18 Class II	1.8V	0.9V
	HSTL18 Class III	1.8V	1.1V
Differential	GTL	--	0.8V
	GTL+	--	1.0V
	LVDS2.5	2.5V	--
	Bus LVDS2.5	2.5V	--
	Ultra LVDS2.5	2.5V	--
	LVDS_ext2.5	2.5V	--
	RS DS	2.5V	--
	LDT2.5	2.5V	--

Xilinx Spartan-3E Family



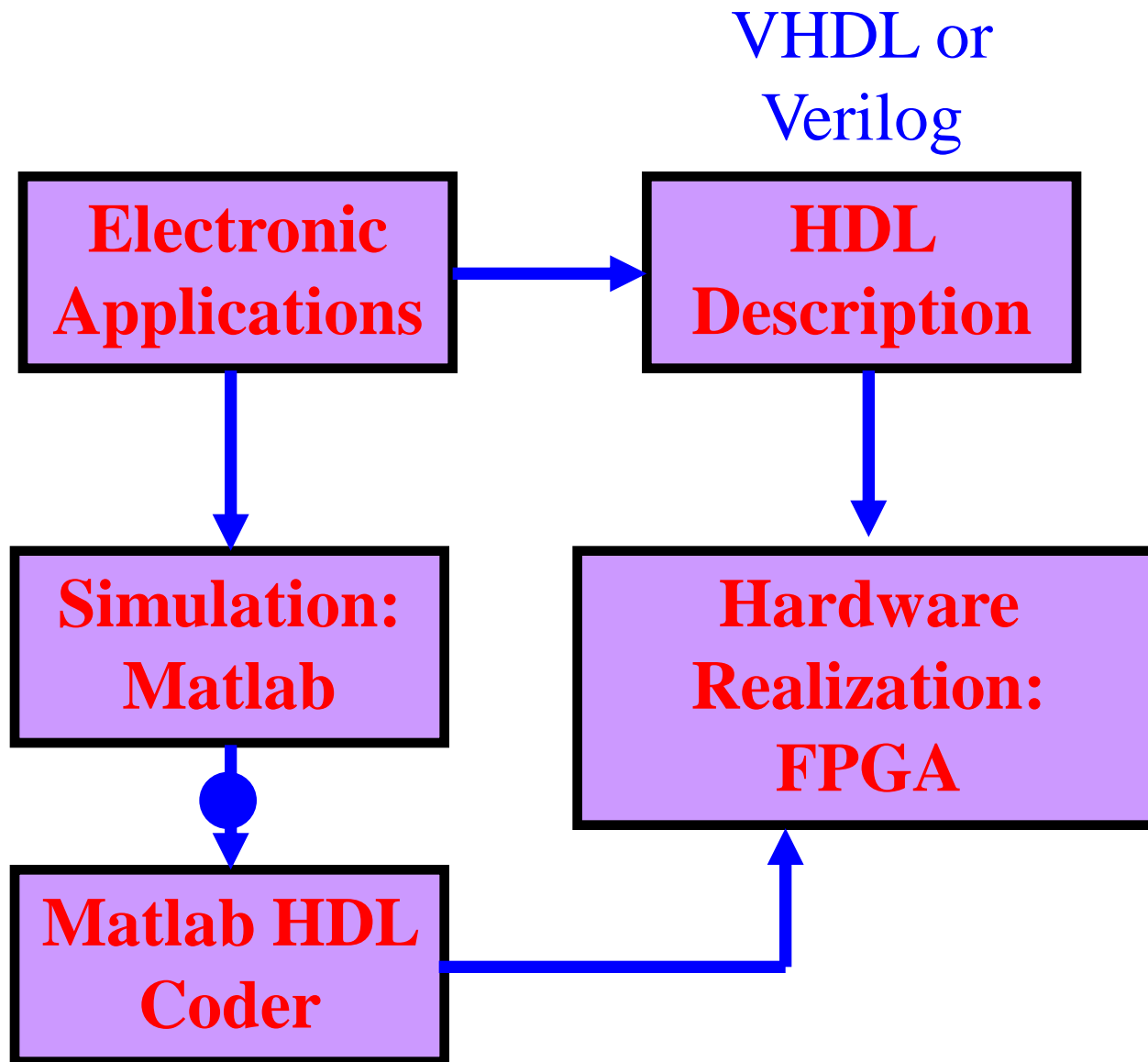
	3S100E	3S250E	3S500E	3S1200E	3S1600E
Device					
Gates	100K	250K	500K	1.2M	1.6M
Logic Cells	2,160	5,508	10,476	19,512	33,192
Maximum I/O	108	172	232	304	376
Block RAM bits	72K	216K	360K	504K	648K
Distributed RAM bits	15K	38K	73K	136K	231K
18x18 Multipliers	4	12	20	28	36
DCMs	2	4	4	8	8

Highly Recommended Books

- **The Design Warrior's Guide to FPGAs**
- **Clive Maxfield**

- **Fundamentals of Digital Logic with VHDL**
- **Stephen Brown, Zvonko Vranesic**

Overview



What You Need?

- **Hardware Description Language:**
 - ◆ VHDL.
 - ◆ Verilog.
- **FPGA:**
 - ◆ Structure.
 - ◆ Download Skills.
 - ◆ Data Transfer Skills.

Thanks